via an internal bus to the program counter register, together with an instruction decode unit which includes a circuit for detecting the presence of a distinguished bit in the 8-bit bytecode, together with a circuit for loading the remaining bits of the bytecode shifted left by a number of bits into the microprocessor's program counter register, while at the same time storing the current value of the program counter register on the aforementioned stack.--

REMARKS

By this Amendment, claims 1-15 have been cancelled without prejudice, and new claims 16-30 have been added. No new matter has been added. Claims 16-30 are submitted for consideration.

Timely examination on the merits is respectfully submitted.

Please charge any fee deficiency or credit any overpayment to Deposit Account No. 01-2300.

Respectfully submitted,

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